|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | RegWrite | RD/IM | Binv | Cin | ALUop | Mem to Reg | RegDest | Branch | Jump | Load | Store |
| sw | 0 | 1 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | 0 | 1 |
| lw | 1 | 1 | 0 | 0 | 00 | 1 | 0 | 0 | 0 | 1 | 0 |
| beq | 0 | 0 | 1 | 1 | 00 | 0 | 1 | 1 | 0 | 0 | 0 |
| addi | 1 | 1 | 0 | 0 | 00 | 0 | 0 | 0 | 0 | 0 | 0 |
| sub | 1 | 0 | 1 | 1 | 00 | 0 | 1 | 0 | 0 | 0 | 0 |
| jmp | 0 | 0 | 0 | 0 | xx | 0 | 0 | 0 | 1 | 0 | 0 |
| and | 1 | 0 | 0 | 0 | 01 | 0 | 1 | 0 | 0 | 0 | 0 |
| slt | 1 | 0 | 0 | 0 | 10 | 0 | 1 | 0 | 0 | 0 | 0 |
| sll | 1 | 0 | 0 | 0 | 11 | 0 | 1 | 0 | 0 | 0 | 0 |
| add | 1 | 0 | 0 | 0 | 00 | 0 | 1 | 0 | 0 | 0 | 0 |

Table of Control Unit